Amendments to the Claims:

This listing of claims will replace all prior version, and listings, of claims in the application. Where claims have been amended and/or canceled, such amendments and/or cancellations are done without prejudice and/or waiver and/or disclaimer to the claimed and/or disclosed subject matter, and the applicant and/or assignee reserves the right to claim this subject matter and/or other disclosed subject matter in a continuing application.

Listing of the claims:

1. (Original) A latency compensation circuit for use in a first wireless access point operating in accordance with a communications protocol comprising: a first acquisition circuit for identifying receipt of a first data packet from a second wireless access point; a speculative response circuit for issuing a speculative response to said first data packet to said second wireless access point; wherein said speculative response is transmitted by said first access point before said first wireless access point has completed a packet decoding operation on said first data packet.

2. (Original) The latency compensation circuit of claim 1, wherein said speculative response is a pre-stored preamble.

3. (Original) The latency compensation circuit of claim 1, wherein said packet decoding operation is associated with a multi-antenna signal processing circuit operating on N separate received data signals, where N>1.

4. (Original) The latency compensation circuit of claim 1, wherein said speculative response is generated to ensure that said first wireless access point complies with timing requirements of said communications protocol.

5. (Original) The latency compensation circuit of claim 4, wherein said timing requirements are

associated with a Short Inter-Frame Spacing (SIFS) interval of an 802.11x compatible data link.

6. (Original) The latency compensation circuit of claim 5, wherein said SIFS interval is less than half a latency time associated with said packet decoding operation.

7. (Original) The latency compensation circuit of claim 1, wherein an acknowledgement transmission packet and a received packet are processed simultaneously.

8. (Original) The latency compensation circuit of claim 1, wherein said first wireless access point is configured in a contention free period (CFP) mode.

9. (Original) The latency compensation circuit of claim 8, wherein said first wireless access point determines an access sequence for a wireless medium with respect to other access points to identify said CFP.

10. (Original) An access radio frequency (RF) multi-antenna access point system comprising: a multi-antenna signal processing circuit situated in a first access point and adapted to: (a) receive M separate data packets from a second access point representing a single multiplexed data stream; (b) process said M separate data packets during a packet decoding operation, which packet decoding operation requires a first time period; (c) generate a packet acknowledgement when a data packet is received, and prior to an expiration of said first time period, so that a processing latency associated with said packet decoding operation does not cause a violation of a timing requirement in a wireless medium used by said first access point.

11. (Original) The circuit of claim 10, wherein said multi-antenna signal processing circuit is enabled and selectively transmits only when channel conditions indicate that a data rate in said channel has fallen below a predetermined threshold.

12. (Original) The circuit of claim 10, wherein said multi-antenna signal processing circuit is enabled and selectively transmits in response to a determination that a data rate in said channel is to be enhanced above a nominal operating rate.

13. (Original) The circuit of claim 10, wherein said multi-antenna signal processing circuit is enabled and selectively transmits in response to a determination that frequency selective fading is present in said channel.

14. (Original) The circuit of claim 10 wherein said multi-antenna signal processing circuit is situated in a signal path ahead of a first baseband processor, and is further adapted to monitor channel transmission conditions to identify whether an operation of said first baseband processor should be enhanced.

15. (Original) The circuit of claim 10, wherein said timing requirement is associated with an 802.11x communications protocol.

16. (Original) The circuit of claim 10 wherein said packet acknowledgement is a dummy data value for a transmission packet preamble.

17. (Original) The circuit of claim 10 wherein said multi-antenna signal processing circuit is configured as a multiple-in, multiple out (MIMO) processor.

18. (Original) The circuit of claim 10, wherein said multi-antenna signal processing circuit demodulates a data stream transmitted using multiple independent antennas which each transmit a portion of said data stream.

19. (Original) A radio frequency (RF) multi-antenna access point system implemented in a single chip integrated circuit chip (IC) comprising: a baseband processor circuit located in a first portion of the single chip IC for handling data transmissions during a first operating mode in a channel between a first access point and a second access point; a multi-antenna signal processing circuit located in a second portion of the single chip IC for handling data transmissions during a second operating mode in said channel, said multi-antenna signal processing circuit being further adapted to: (a) receive M independent RF modulated input signals from said second access point; (b) process said M independent RF modulated input signals using a channel mixing matrix to extract N independent data signals transmitted by said second access point; wherein said first operating mode and said second operating mode are automatically selected by the RF multi-antenna access point system based on a transmission condition in said channel; (c) generate a transmission acknowledgement when said M independent RF modulated data signals are received, and prior to an expiration of step (b) so that a processing latency of said multi-antenna signal processing circuit does not cause a violation of a timing requirement in a wireless medium used by said first access point.

20. (Original) The RF multi-antenna access point system of claim 19, wherein said multi-antenna signal processing circuit includes an analog to digital converter, and a digital to analog converter for interfacing to an antenna.

21. (Original) The RF multi-antenna access point system of claim 20, wherein said multi-antenna signal processing circuit includes a Fast Fourier Transform (FFT) Circuit.

22. (Original) The RF multi-antenna access point system of claim 21, wherein said multi-antenna signal processing circuit includes a preamble acquisition circuit for performing a preamble acquisition to align an FFT data frame with an 802.11x based data stream. (Previously Presented)

23. (Original) The RF multi-antenna access point system of claim 19, wherein said multi-antenna signal

processing circuit processes at least 4 separate input signals representing a data stream multiplexed over 4 separate bit streams.

24. (Original) The RF multi-antenna access point system of claim 19, wherein said channel mixing matrix performs an operation that computes a recovered data signal x as follows: x=b1*y1+b2*y2+x0 where b1 and b2 are equalization coefficients computed by said multi-antenna signal processing circuit, y1 and y2 are received data from separate baseband channels, and x0 is a recovered signal from an adjacent channel.

25. (Original)The RF multi-antenna access point system of claim 19, wherein space division multiple access is realized by separating different RF signals from different signal paths simultaneously in the single chip IC.

26. (Original)The RF multi-antenna access point system of claim 19, wherein said multi-antenna signal processing circuit extends a data transmission range achieved by said baseband processor circuit between said first access point and said second access point.

27. (Original)The RF multi-antenna access point system of claim 19, wherein said multi-antenna signal processing circuit increases a data transmission rate achieved by said baseband processor circuit between said first access point and said second access point.

28. (Original)The RF multi-antenna access point system of claim 19, wherein said multi-antenna signal processing circuit transmits M separate data signals to said second access point.

29. (Original)The RF multi-antenna access point system of claim 28, wherein a localized encryption is achieved for said second access point by independently controlling said M separate transmission signals.

30. (Original) The circuit of claim 19, wherein said timing requirement is associated with an 802.11x communications protocol.

31. (New) A circuit for use in a first access point comprising:

a first circuit capable of identifying receipt of a first data packet;

a second circuit capable of issuing a response to the first data packet; and

wherein the response is capable of being transmitted by the first access point before the first access point has completed a packet decoding operation on the first data packet.

32. (New) A circuit according to claim 31, wherein the response comprises a pre-stored preamble.

33. (New) A circuit according to claim 31, wherein the packet decoding operation is associated with a multi-antenna signal processing circuit operating on N separate received data signals, where N>1.

34. (New) A circuit according to claim 31, wherein the response is generated to ensure that the first wireless access point complies with timing requirements of a communications protocol.

35. (New) A circuit according to claim 34, wherein the timing requirements are associated with a Short Inter-Frame Spacing (SIFS) interval of an IEEE 802.11 type compatible data link.

36. (New) A circuit according to claim 35, wherein the SIFS interval is less than half a latency time associated with the packet decoding operation.

37. (New) A circuit according to claim 31, wherein an acknowledgement transmission packet and a received first data packet are processed simultaneously or nearly simultaneously.

38. (New) A circuit according to claim 31, wherein the first wireless access point is capable of being configured in a contention free period (CFP) mode.

39. (New) A circuit according to claim 38, wherein the first wireless access point is capable of determining an access sequence for a wireless medium with respect to other access points to identify the CFP.

40. (New) A system for use in a first access point comprising:

a mobile terminal for communicating with at least a first access point;

a first circuit capable of identifying receipt of a first data packet;

a second circuit capable of issuing a response to the first data packet; and

wherein the response is capable of being transmitted by the first access point before the first access point has completed a packet decoding operation on the first data packet.

41. (New) A multi-antenna access point system comprising:

a mobile terminal capable of communicating with a first access point;

a multi-antenna signal processing circuit situated in a first access point capable of:

receiving M separate data packets from a second access point;

processing the M separate data packets during a packet decoding operation in a first time period; and

generating a packet acknowledgement prior to an expiration of the first time period when a data packet is received.

42. (New) A multi-antenna access point system according to claim 41, wherein the multi-antenna signal processing circuit is capable of transmitting if channel conditions indicate that a data rate in the channel has fallen below a predetermined threshold.

43. (New) A multi-antenna access point system according to claim 41, wherein the multi-antenna signal processing circuit is capable of transmitting in response to a determination that a data rate in the channel is to be enhanced above a nominal operating rate.

44. (New) A multi-antenna access point system according to claim 41, wherein the multi-antenna signal processing circuit is capable of transmitting in response to a determination that frequency selective fading is present in the channel.

45 (New) A multi-antenna access point system according to claim 41, wherein the multi-antenna signal processing circuit is situated in a signal path ahead of a first baseband processor, and is further capable of monitoring channel transmission conditions to identify whether an operation of the first baseband processor should be enhanced.

46. (New) A multi-antenna access point system according to claim 41, further comprising a timing requirement associated with an IEEE 802.11 type communications protocol.

47. (New) A multi-antenna access point system implemented in a single chip integrated circuit chip (IC) comprising:

a baseband processor circuit located in a first portion of the single chip IC capable of handling data transmissions during a first operating mode in a channel between a first access point and a second access point; and

a multi-antenna signal processing circuit located in a second portion of the single chip IC capable of handling data transmissions during a second operating mode in the channel.

48. (New) A multi-antenna access point system according to claim 47, the multi-antenna signal processing circuit further capable of:

receiving M independent modulated input signals from the second access point; and

processing the M independent modulated input signals.

49. (New) A multi-antenna access point system according to claim 47, wherein the first operating mode or the second operating mode are selected by the multi-antenna access point system based at least in part on a transmission condition in the channel.

50. (New) A multi-antenna access point system according to claim 47, further capable of generating a transmission acknowledgement if the M independent modulated data signals are received, and prior to an expiration of step such that a processing latency of the multi-antenna signal processing circuit does not cause a violation of a timing requirement in a wireless medium used by the first access point.

51. (New) An apparatus comprising:

means for identifying receipt of a first data packet;

means for issuing a response to the first data packet; and

means for transmitting a response before decoding the first data packet.

52. (New) An apparatus according to claim 51, wherein the means for transmitting a response further comprises means for transmitting a pre-stored preamble.

53. (New) An apparatus according to claim 51, wherein means for decoding is associated with a multi-antenna signal processing circuit operating on N separate received data signals, where N>1.

54. (New) An apparatus according to claim 51, wherein means for transmitting a response further comprises means for complying with timing requirements of a communications protocol.

55. (New) An apparatus for use in a first access point comprising:

means for communicating with at least a first access point;

means for identifying receipt of a first data packet;

means for issuing a response to the first data packet; and

means for transmitting a response before decoding the first data packet.

56. (New) An apparatus comprising:

means for communicating with a first access point;

means for receiving M separate data packets from a second access point;

processing the M separate data packets during a packet decoding operation in a first time period; and

means for generating a packet acknowledgement prior to an expiration of a first time period when a data packet is received.

57. (New) A method comprising:

identifying receipt of a first data packet;

issuing a response to the first data packet; and

transmitting a response before decoding the first data packet.

58. (New) A method according to claim 57, wherein transmitting a response further comprises transmitting a pre-stored preamble.

59. (New) A method according to claim 57, wherein decoding is associated with a multi-antenna signal processing circuit operating on N separate received data signals, where N>1.

60. (New) A method according to claim 57, wherein transmitting a response further comprises complying with timing requirements of a communications protocol.

61 (New) A method for use in a first access point comprising:

communicating with at least a first access point;

identifying receipt of a first data packet;

issuing a response to the first data packet; and

transmitting a response before decoding the first data packet.

62. (New) A method comprising:

communicating with a first access point;

receiving M separate data packets from a second access point;

processing the M separate data packets during a packet decoding operation in a first time period; and

generating a packet acknowledgement prior to an expiration of a first time period when a data packet is received.